

ACTIVE WAFER FOR IMPROVED GIGABIT SIGNAL
RECOVERY, IN A SERIAL POINT-TO-POINT
ARCHITECTURE

BACKGROUND OF THE INVENTION

[0001] Embodiments of the present invention generally relate to an electrical connector for use with point-to-point serial data streams and particularly to connectors that compensate for signal loss within point-to-point data streams.

[0002] In the past, right angle connectors have been provided for connection between printed circuit boards. The right angled connectors may use a large plurality of receiving terminals oriented at a right angle to an equally large plurality of pins. One common implementation of such connectors is to join daughter cards with a backplane in a data transmission system. In conventional systems, connectors have been proposed that are able to support bi-directional data streams arranged in a multi-drop bus configuration. These conventional bi-directional data streams conveyed signals in opposite directions over each individual trace through the connector.

[0003] Existing multi-drop bus architectures utilize a single driver or transmitter, such as arranged on one daughter card that transmits a signal along a trace along the backplane. This trace on the backplane is tapped at multiple locations to feed a plurality of receivers on an equal plurality of daughter cards. Hence, a single transceiver (transmitter/receiver) on a first daughter card may communicate along a common trace over the backplane to a plurality of transceivers arranged on separate other daughter cards.

[0004] However, conventional configurations have experienced certain disadvantages at high data rates. As the data rate increases, the high frequency components of the signal experience more loss and more reflection within the backplane and connector assemblies interconnecting the daughter cards. Signal degradation increases as the number of daughter cards increases that tap into a single trace along the backplane. For example, as the data rate increases, each signal trace, within an individual connector extending to the daughter cards,

begins to function more as a transmission line. As the traces extending to each daughter card exhibit more characteristics of transmission lines, the energy conveyed along the backplane divides at each point where a daughter card connector tapped into a trace on the backplane. The more times the energy is split, the more reflection and loss is experienced. Conventional connectors have attempted to reduce the negative effects of the multi-drop bus architecture by providing a bus arbitration logic chip as a switch within a bi-directional communications link. One example of such a configuration is illustrated in U.S. Patent 6,168,469.

[0005] However, bi-directional communication format and multi-drop bus architectures continue to exhibit signal degradation and reliance problems. Hence, bi-directional communications and multi-drop bus architectures are becoming less frequently used and are no longer desirable in certain applications. Instead, an entirely different communications format and connector architecture are now being advanced, namely serial communication over a point-to-point architecture. In serial communication over a point-to-point architecture, each transmitter is uniquely associated with a single receiver to afford a distinct and separate communications link therebetween. In a point-to-point architecture, only as single daughter card taps into a single trace along the backplane. Each transmitter and receiver upon each daughter card is afforded a dedicated communications path and dedicated traces both within the connector and along the backplane. Conventional approaches, such as described in the '469 patent, are not useful nor afford any advantage in point-to-point architectures.

[0006] Hence, a need remains for an improved connector assembly designed for a point-to-point architecture that conveys serial data streams.

BRIEF DESCRIPTION OF THE INVENTION

[0007] An electrical connector is provided for connection to a point-to-point architecture. The connector includes an insulated housing having first and second card interfaces configured to mate with associated first and second circuit cards. An electrical wafer is held in the housing and configured to interconnect circuit boards in a point-to-point architecture. The wafer has first and second interfaces. The wafer has signal traces that end at input and output contact pads located proximate to first and second interfaces, respectively. The input contact

pads receive a serial signal, while the output contact pads transmit the serial signal. Each of the signal traces include a first break at an intermediate point along a length thereof to form a disconnect in the signal traces. The connector further includes an active compensation component bridging the first breaks in the signal traces. The active compensation component compensates for signal degradation within the point-to-point architecture for the signal incoming from the input contact pads and transmits a compensated signal outward to the output contact pads. The active compensation component transmits the signal only in a single direction within the point-to-point application.

[0008] Optionally, the active compensation component may include preemphasis signal conditioning for conditioning the signal incoming from the input contact pads. The preemphasis signal conditioning increases, within a band of frequencies, a magnitude of higher frequency components of the signal with respect to a magnitude of lower frequency components of the signal.

[0009] The wafer also includes one or more power contact pads thereon. Optionally, the power contact pads may be located at one of the interfaces, while a power trace extends from the contact pad to the active compensation circuit. Optionally, the wafer may be configured such that the active compensation component and the power contact pad are located on a first side of the wafer, while a power trace is located on the second side of the wafer with the power trace interconnecting the power contact pad and the active compensation component through vias extending through the wafer.

[0010] As a further option, passive signal compensation components may be provided on the wafer in addition to the active compensation components. The passive signal compensation components may be provided upstream of the active compensation component such that the passive signal components are located between the input contact pads and the active compensation component. The passive signal compensation components may perform various signal conditioning functions including filtering among others.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 illustrates an expanded isometric view of a connector assembly formed in accordance with an embodiment of the present invention.

[0012] Figure 2 illustrates an isometric view of a backplane assembly having a contact pulled outward therefrom in accordance with an embodiment of the present invention.

[0013] Figure 3 illustrates one side of a wafer formed in accordance with an embodiment of the present invention.

[0014] Figure 4 illustrates an opposite side of the wafer of Figure 3.

[0015] Figure 5 illustrates one side of a wafer formed in accordance with an alternative embodiment of the present invention.

[0016] Figure 6 illustrates an opposite side of the wafer of Figure 5.

DETAILED DESCRIPTION OF THE INVENTION

[0017] Figure 1 illustrates a connector assembly 10 formed in accordance with an embodiment of the present invention. The connector assembly 10 includes a housing which includes an L-shaped frame 14 and an h-shaped cover 16 that mate with one another. The frame 14 includes a lower face that defines a daughter card interface 18 formed integrally with a backwall 20. The cover 16 comprises a top wall 21 formed integrally with a front wall defining a backplane assembly interface 22. The backplane assembly interface 22 includes upper and lower flanges 24 and 26 extending outward from the backplane assembly interface 22 to define a contact mating area (generally denoted by reference numeral 28). The frame 14 and cover 16 receive and retain a plurality of cards or wafers 30 which are arranged parallel to one another and spaced apart from one another. Optionally, the wafers 30 may be separated by ground shields (not shown). Each wafer 30 includes an edge defining a backplane edge 32 which extends through slots formed in the backplane assembly interface 22. The backplane edge 32 of each wafer 30 is provided with a series of ground and signal contact pads 36 and 38 arranged in a predefined sequence.

[0018] As shown in Figure 1, the signal contact pads 38 are provided along one side of each wafer 30. The signal contact pads 38 are further arranged in differential pairs (one example of which is denoted by bracket 40), where each differential pair 40 of signal contact pads 38 is separated by a ground contact pad 36. The ground contact pads 36 are formed longer than the signal contact pads 38 to extend outward to the backplane edge 32. The signal contact pads 38 are positioned on the wafer 30 spaced slightly inward and from the backplane edge 32.

[0019] With reference to the daughter card interface 18, a series of positioning pins (not shown) are provided and are received in holes in a mating daughter card to facilitate alignment therebetween. The daughter card interface 18 includes a plurality of holes 44 through which contacts 46 project. The upper ends (not shown) of the contacts 46 mate with contact pads on the wafer 30 as explained below in more detail. The ends of the contacts 46 extending downward from the daughter card interface 18 are configured to be received in vias or through holes provided in a daughter card mated with the connector assembly 10.

[0020] Figure 2 illustrates a backplane assembly 50 configured to be joined with the daughter card assembly 10 (Fig. 1). The backplane assembly 50 includes a front face 52 which fits in and mates with the contact mating area 28 (Fig. 1) of the backplane assembly interface 22 on the connector assembly 10. The backplane assembly 50 includes a back face 54 that is configured to be secured to a backplane printed circuit board (not shown). The backplane assembly 50 retains a plurality of contacts 56. Each contact 56 includes an eye of the needle contact tip 58 at one end and a dual beam tip 60 at the opposite end. When the backplane assembly 50 is mated with the connector assembly 10, the dual beam tips 60 press against corresponding ground and signal contact pads 36 and 38 on respective wafers 30.

[0021] Figures 3 and 4 illustrate opposite sides of a wafer 30 formed in accordance with an embodiment of the present invention. For purposes of explanation only, the side illustrated in Figure 3 will be referred to as the front side 62, while the side illustrated in Figure 4 will be referred to as the back side 64. With reference to Figure 3, the wafer 30 includes a backplane interface edge 32 oriented at a right angle to a daughter card interface edge 66. Optionally, the backplane and daughter card interface edges 32 and 66 may be oriented at acute or obtuse angles with respect to one another (or opposing one another at 180° angle). The wafer

30 also includes top and back edges 68 and 70, respectively. The front side 62 of the wafer 30 is formed with multiple ground plane sections 72 which are spaced apart to separate signal traces 74 that are arranged in differential pairs in the example of Figure 3. The signal traces end at signal contact pads 38 proximate the backplane edge 32. The traces 74 also end at signal contact pads 78 proximate the daughter card interface edge 66.

[0022] The wafer 30 is configured to support a serial or uni-directional data stream within a point-to-point architecture, in which data signals are conveyed in a single direction through each signal trace 74. Hence, each individual signal contact pad 38 either only receives or only transmits signals within the entire point-to-point architecture, while the signal contact pads 78 operate in the exact opposite manner. Accordingly, individual signal contact pads 38 are configured as dedicated transmit or dedicated receive contact pads. By way of example only, a signal contact pad 38 may represent a dedicated receive or input contact pad that only receives serial signals, in which case the interconnected signal contact pad 78 will only and always operate as a dedicated transmit or output contact pad to transmit the serial signal.

[0023] The signal contact pads 78 are grouped into differential pairs 80, each of which is separated by ground contact pads 82. In addition, a power contact pad 84 is provided proximate the daughter card interface edge 66. The power contact pad 84 is joined at a via or through-hole 86 to a trace on the back side 64 of the module 30.

[0024] It is understood that while a first differential pair 76 of signal traces 74 support serial signal transmission in a first direction, a separate and distinct differential pair 76 of signal traces 74 on the same wafer 30 may support a different serial signal transmitting in the opposite direction. Hence, a first set of differential pairs 80 along the daughter card interface edge 66 may represent output contact pads, while a different differential pair 81 of signal contact pads 78, also along the daughter card interface edge 66, may constitute input contact pads.

[0025] In the example of Fig. 3, two differential pairs 76 of signal traces 74 include break sections 88 provided at intermediate points along the lengths of the signal traces. The break sections 88 form a disconnect in the signal traces 74 in which the break sections 88 are positioned. A component reception area 90, as denoted by a dashed line, surrounds each of

the break sections 88. The component reception area 90 includes an arrangement of flared ends 91 on each signal trace 74. The flared ends are located proximate a gap 106. Component pads 92 are located across the gap 106 from the flared ends 91. Capacitors resistors and the like (generally denoted by reference numeral 93) may be provided to bridge the gap 106. By way of example, a capacitor 93 may be provided as a DC blocking capacitor bridging the gap 106 between a corresponding flared end 91 and component pad 92. Optionally, the capacitors, resistors and the like 93 and the gap 106 may be removed, such that the flared ends 91 of each signal trace 74 extend into and directly join with the active compensation component 94. In the example of Fig. 3, the active signal compensation component 94 includes pins that join the narrow portions of corresponding component pads 92 (for example, generally in line between the power pads 98). Individual signal traces 74 are divided into discrete and separate sections where each section is formed with flared end 91 at one end and either one of the signal contact pads 38 and 78 at the other end or another component pad 92.

[0026] An active compensation component 94 is illustrated as bridging one break section 88 in one differential pair 76 of signal traces 74. Optionally, a single active compensation component 94 may bridge breaks for multiple signals and/or differential pairs. The active compensation component 94 supports unidirectional signals in a point-to-point architecture. The active compensation component 94 compensates single-ended or differential signals that are incoming (by way of example) from the input contact pads (for example the signal contact pads 78). The active compensation component 94 compensates for signal degradation caused by the point-to-point architecture and outputs a corresponding single-ended or differential signal to the output contact pads (signal contact pads 38). The active compensation component 94 only transmits signals in a single direction, and does not support bi-directional communication over the signal traces 74. The active compensation component 94 receives power from power pads 98 which are joined, through vias 100, to power traces on the back side 64 of the wafer 30.

[0027] Active and/or passive components may perform signal compensation. The terms “signal compensation” and “compensation” are used broadly throughout the present application to refer to compensation for signal degradation in a system or point-to-point architecture. Signal degradation may be comprised of one or more of transmission medium

losses, structural resonances, noise, radiation, jitter and the like. Examples of the functions that may be performed by active or passive signal compensation components include equalization, pre-emphasis, buffering/amplification, retiming, error correction and/or clock-data recover.

[0028] Optionally, the active compensation component 94 may perform amplification based upon a gain curve that is inversely associated with a loss curve corresponding to the particular configuration of signal traces 74 in use. The loss curve will vary between different wafers 30 depending upon the pattern of signal traces 74. The active compensation component 94 may adjust the gain introduced into the differential signals based on the level of power input to the active compensation component 94. Hence, remote control is afforded over the amount of gain by adjusting the power input. In addition, the active compensation component may include preemphasis functionality. The term “preemphasis” is used to refer to a process to define, within a band of frequencies, a magnitude of select frequencies (e.g. high frequency components) with respect to the magnitude of other select frequencies (e.g. lower frequency components). Preemphasis may improve the overall signal to noise ratio by reducing the adverse effects of certain phenomena such as attenuation differences in other parts of the system. Preemphasis may be used in part to account for the fact that high frequency components of the signals being conveyed through the signal traces 74 are attenuated to a more significant degree than low frequency components.

[0029] Optionally, the active compensation component 94 may simply constitute an equalizer or a repeater circuit.

[0030] Figure 4 illustrates the back side 64 of the wafer 30. The back side 64 includes one or more of ground plane sections 96 arranged to substantially cover a majority of the back side 64. The back side 64 also includes a power trace 102 that extends from the daughter card interface edge 66 along the back edge 70 to the top edge 68. The power trace 102 extends in a curved manner to regions of the back side 64 directly across from and in alignment with the component reception areas 90 (Fig. 3). The power trace 102 is separated from the ground plane section 96 by a thin discontinuity 106 in the conductive materials. The ground plane sections 72, signal traces 74, component pads 92 and power pads 98 are separated by a disconnect 106 (Figs. 3 and 4) in the conductive material. The power trace 102 interconnects

with vias 100. The vias 100 interconnect the power trace 102 on the back side 64 (Fig. 4) with the power pads 98 on the front side 62 (Fig. 3).

[0031] The active compensation components 94 and the wafers 30 are designed and configured to convey single-ended or differential signals at very high data rates, such as 5 gigabits per second or more and up to 10 gigabits per second, or even higher.

[0032] Figures 5 and 6 illustrate an alternative embodiment for a wafer 130. The wafer 130 includes a front side 162 (Fig. 5) and a back side 164 (Fig. 6). The wafer 130 includes ground plane sections 172 on the front side 162 which separate signal traces 174. Signal traces 174 include break sections 188 that form a disconnect. The break sections 188 are surrounded by component pads 192 and power pads 198 which join with corresponding signal and power pins on an active compensation component (not shown in Fig. 5). The signal traces 174 extend between signal contact pads 178 proximate the daughter card interface edge 166 and signal contact pads 138 proximate the backplane edge 132.

[0033] In the embodiment of Figures 5 and 6, an alternative configuration is provided for introducing the power source onto the wafer 130. The embodiment of Figures 5 and 6 does not include a power contact proximate the daughter card interface edge 166. Instead, a pair of power jumper contacts 184 are provided proximate the top edge 168 of the wafer 130. The power jumper contact pads join, through vias 186, to a power trace 202 (Fig. 6) provided on the back side 164 of the wafer 130. The power trace 202 extends from the top edge 168 downward at an intermediate point within the wafer 130 remote from the back side 164 in a somewhat S-shaped pattern. The power trace 202 joins with vias 204 located within the component reception area 190 (Fig. 5), but shown on the back side 164. The vias 204 join the power trace 202 on the back side 164 with power pads 198 on the front side 162.

[0034] As also illustrated in Figure 5, each signal trace 174 may include more than one disconnect or break at flared ends 197. A second break section 189 is illustrated proximate the signal contact pads 138. The break section 189 may be configured to receive separate passive signal compensation components 197. The passive signal compensation components may be capacitors, resistors, inductors and the like, or combinations thereof. For

each signal trace 174, the passive signal conditioning components 191 bridge between component pads 193 and 195 provided on opposite sides of the break section 189. The passive signal conditioning components 191 may filter the signals.

[0035] In accordance with at least one embodiment, active components are provided on the wafers to recover a serial data stream within a point-to-point architecture. By placing the active components on the wafer, the system length, and proportionally the loss, are divided into smaller stages which are more easily recovered. In addition, resonance between the backplane and daughter card plated through holes is interrupted. Signal losses are compensated, and a low cost method for signal recovery is provided.

[0036] Optionally, the power contact pad may be located proximate the backplane edge, top edge or back edge of the wafer.

[0037] Optionally, the wafers 30 may be modified to comprise a lead frame structure in which traces 74 are replaced with a lead frame arrangement. In the lead frame arrangement, the traces represent separate leads held within a chicklet or module which constitutes a wafer. The terms “trace” and “wafer” as used throughout may include “leads” and “chicklets,” respectively.

[0038] Optionally, the wafers 30 may be configured to operate in a single-ended application, not in differential pairs.

[0039] While the invention has been described in terms of various specific embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the claims.